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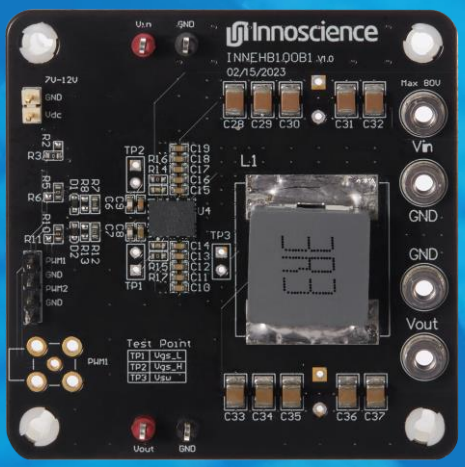
POWER THE FUTURE

INNEHB100B1

Evaluation Board Manual

100V SolidGaN ISG3201

Open Loop EVB



CAUTION

Please carefully read the following content since it contains critical information about safety and the possible hazard it may cause by

ELECTRICAL SHOCK HAZARD

There is a dangerous voltage on the demo board, and exposure to high voltage may lead to safety problems such as injury or death.

Proper operating and safety procedures must be adhered to and used only for laboratory evaluation demonstrations and not directly to end-user equipment.

HOT SURFACE

The surface of PCB can be hot and could cause burns. DO NOT TOUCH THE PCB WHILE OPERATING!!

REMINDER

This product contains parts that are susceptible to electrostatic discharge (ESD). When using this product, be sure to follow antistatic procedures.

List of Content

1. Overview

1.1. Introduction

INNEHB100B1 is a half-bridge evaluation board to evaluate the performance of the fully integrated SolidGaN ISG3201, which integrates two 100V 3.2mohm enhancement mode GaN devices with a 100V half-bridge gate driver. This board simplifies the test process and easily realize Buck converter with single or dual PWM input. The evaluation board can be used in BUCK mode and the efficiency can reach 96.7% at the frequency of 350 kHz, with 48V step-down to 12V at full load 25A with the airflow speed of 1400LFM. The board can also be used in BOOST mode. The board includes the necessary information, and the layout has been optimized to achieve best performance. Test points are also provided for the easy waveform measurement and efficiency evaluation.

1.2. Test Equipment Requirement

To evaluate the performance properly, you need to prepare the following test equipment:

1) High speed digital oscilloscope（≥500MHz Bandwidth）
2) Two low voltage DC power supply
3) PWM generator
4) Digital multimeter
5) DC load (E-load or Power Resistor)

2. Performance summary

Table 1 Electrical Characteristic (Ta=25℃)

Symbol	Parameters	Min	Nom	Max	Units
VDD	VDD supply Voltage	7	8	12	V
Vin	Input Voltage	36	48	80(1)	V
Fsw	Switching frequency		350		kHz
Pout	Output Power			276(2)	W
Eff	Typical efficiency		96.7(3)		%
Vpwm	Input Logic 'High'	3.5		5	V
	Input Logic 'Low'	0		0.8	V

(1) Maximum ringing voltage of switch node must be kept under 100 V for ISG3201.

(2) Maximum power output depends on a variety of factors, including the switching frequency, bus voltage, load current, EVB temperature, and thermal cooling.

(3) 96.7% is the efficiency at 48V to 12V, load current of 25A, switching frequency of 350kHz, and airflow speed of 1400LFM.

3. Block Diagram

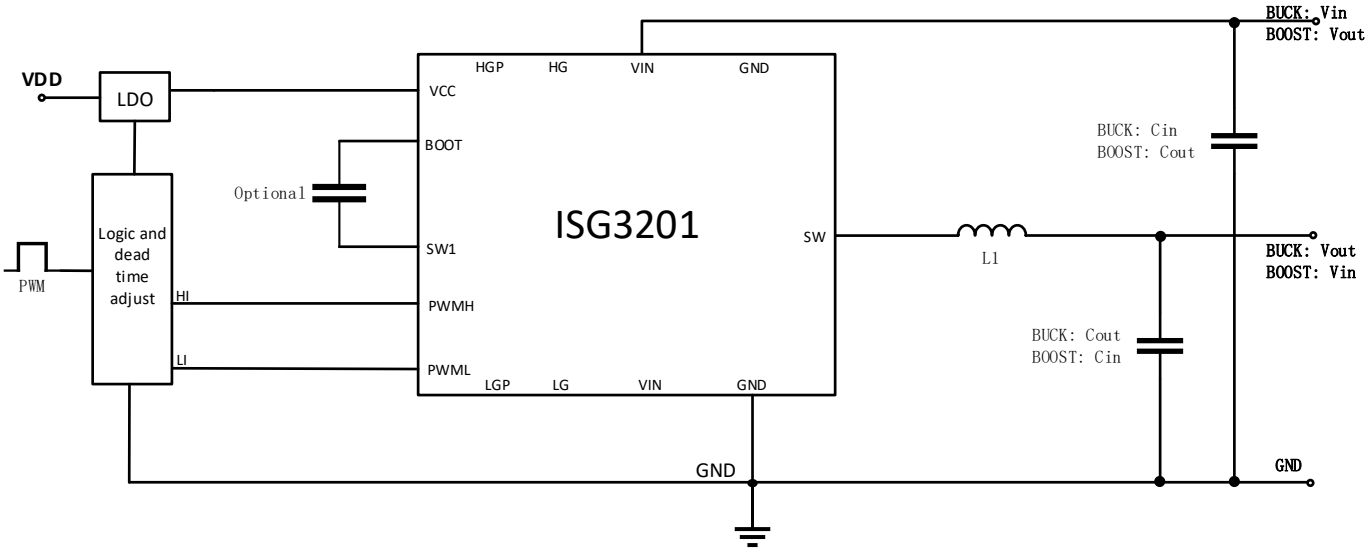


Figure 1 INNEHB100B1 Block Diagram

4. EVB Overview and Schematic

4.1. EVB Overview

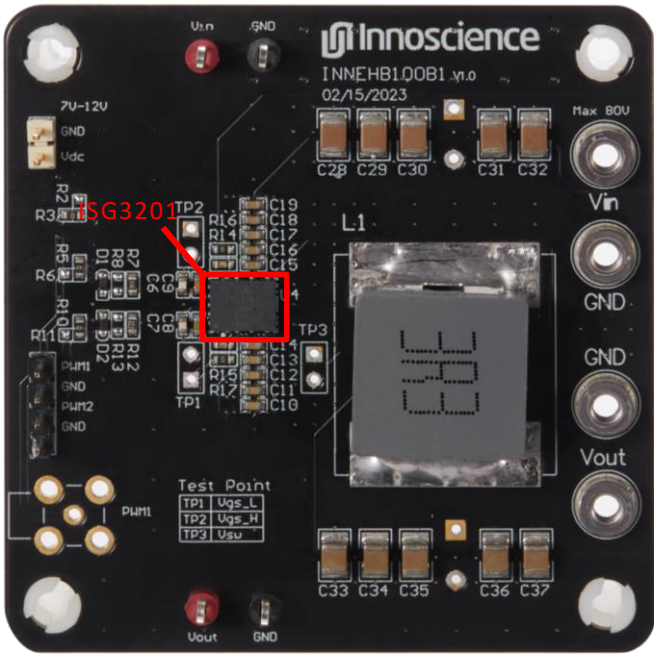


Figure 2 Top view of INNEHB100B1

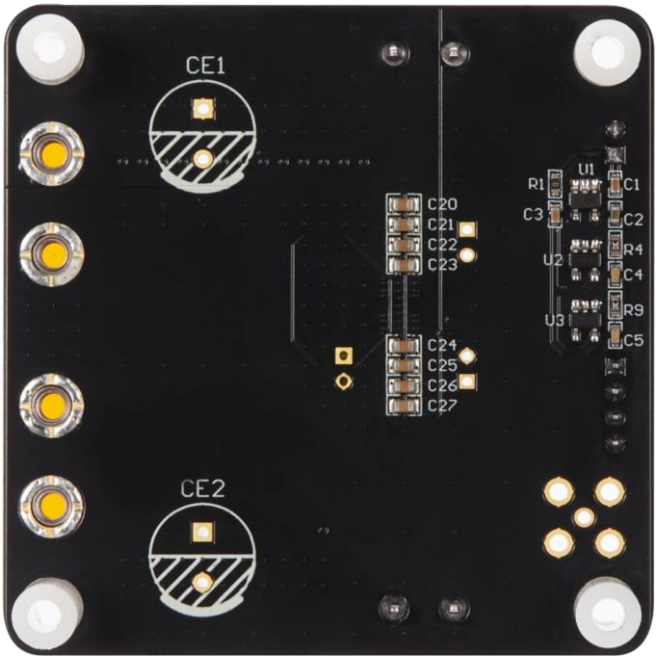


Figure 3 Bottom view of INNEHB100B1

4.2. Schematic

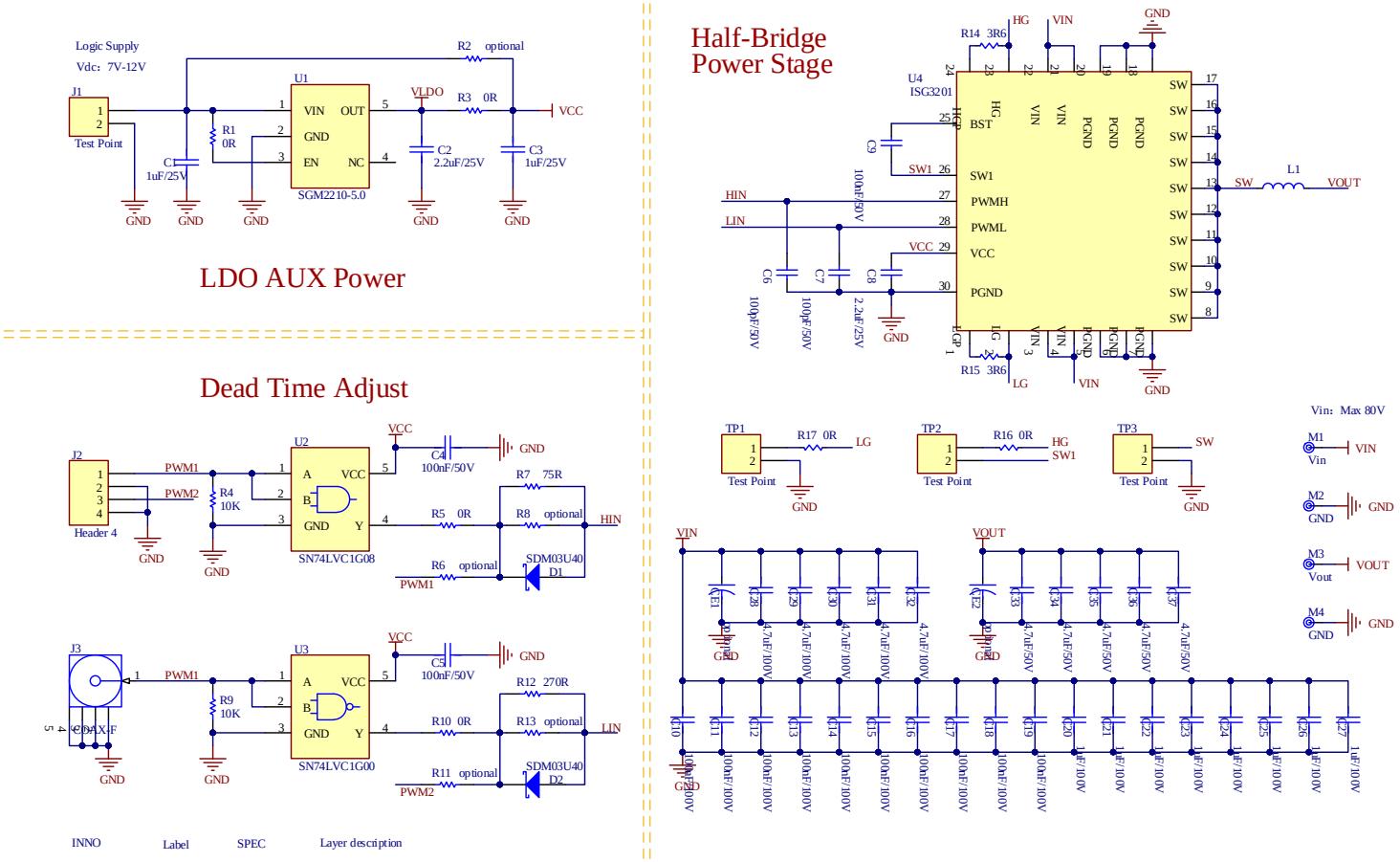


Figure 4 Schematic

5. Testing Guide

5.1. Test point location

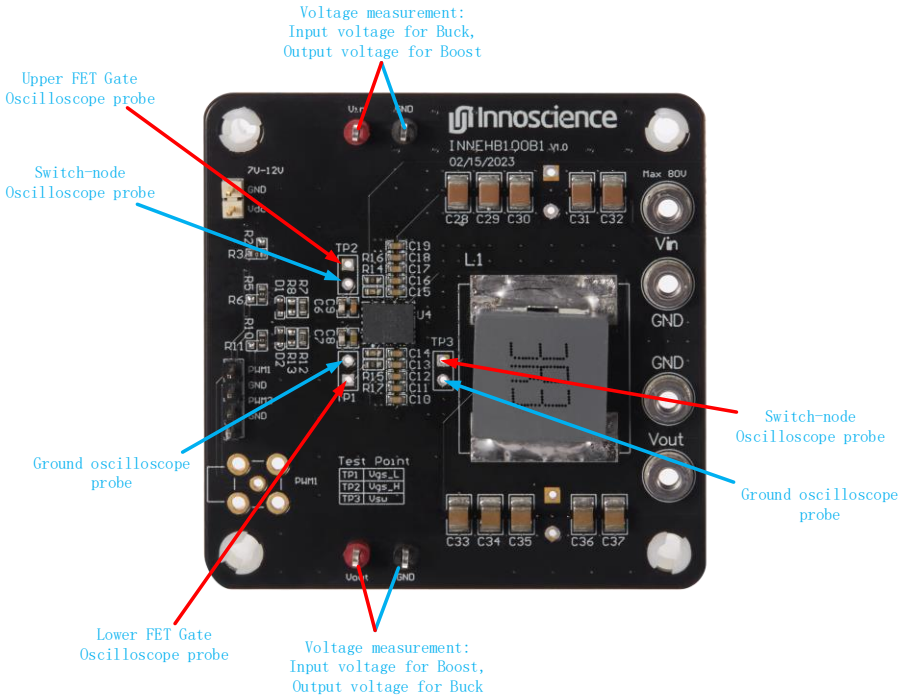


Figure 5 Measurement points

5.2. Test setup

5.2.1. Buck Mode

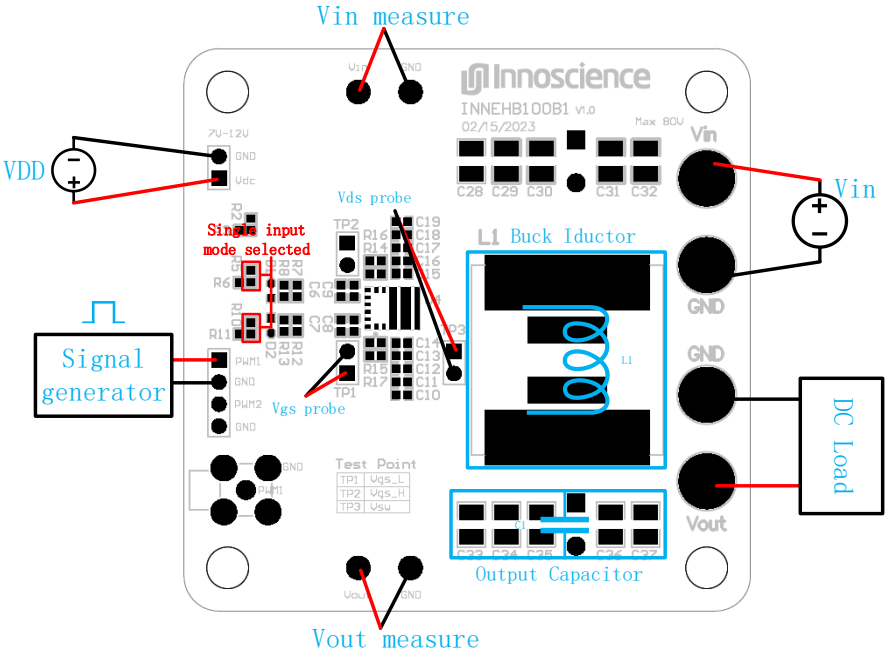


Figure 6 Single-PWM input Buck mode

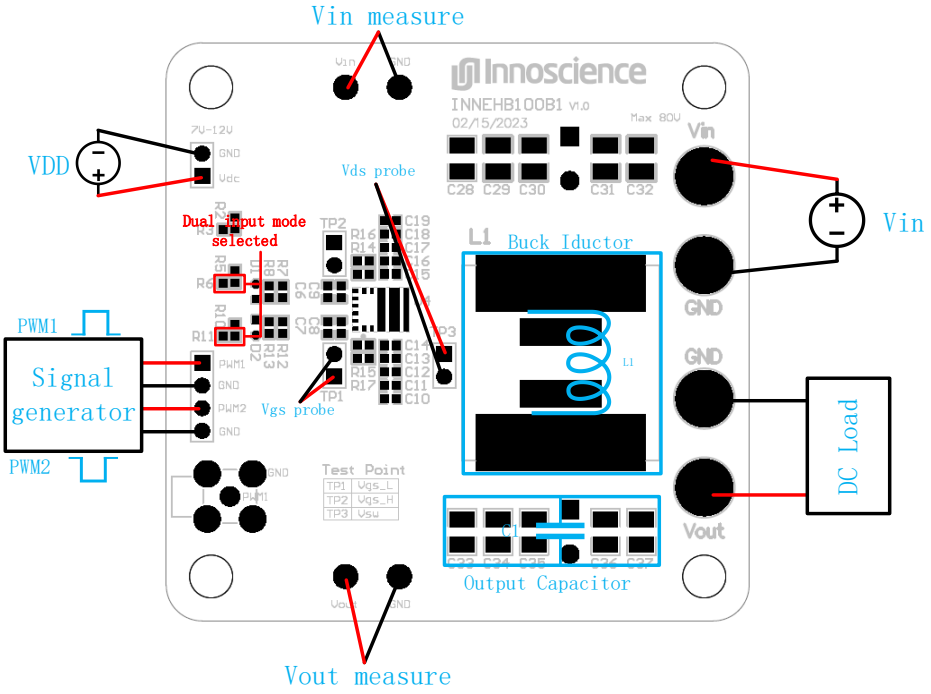


Figure 7 Dual-PWM input Buck mode

Before testing, the single or dual PWM input modes should be selected, R5 & R10 should be 0Ω to select the single PWM input mode. The dead time is regulated by R7, R12, C6 and C7. The value for R7 is 75Ω, and R12 is 270Ω. The values of C6 and C7 are both 100 pF. Under the load of 10A, the measured dead time between low-side GaN turn-off and high-side GaN turn-on is about 3ns. The dead time between high-side GaN turn-off and low-side GaN turn-on is also about 3ns.

To select dual PWM mode, R6, R8, R11 and R13 should be set as 0Ω. Fig. 7 shows the required PWM signals, in which PWM1 and PWM2 should be complementary and he dead time is regulated by the signal generator.

5.2.2. Boost Mode

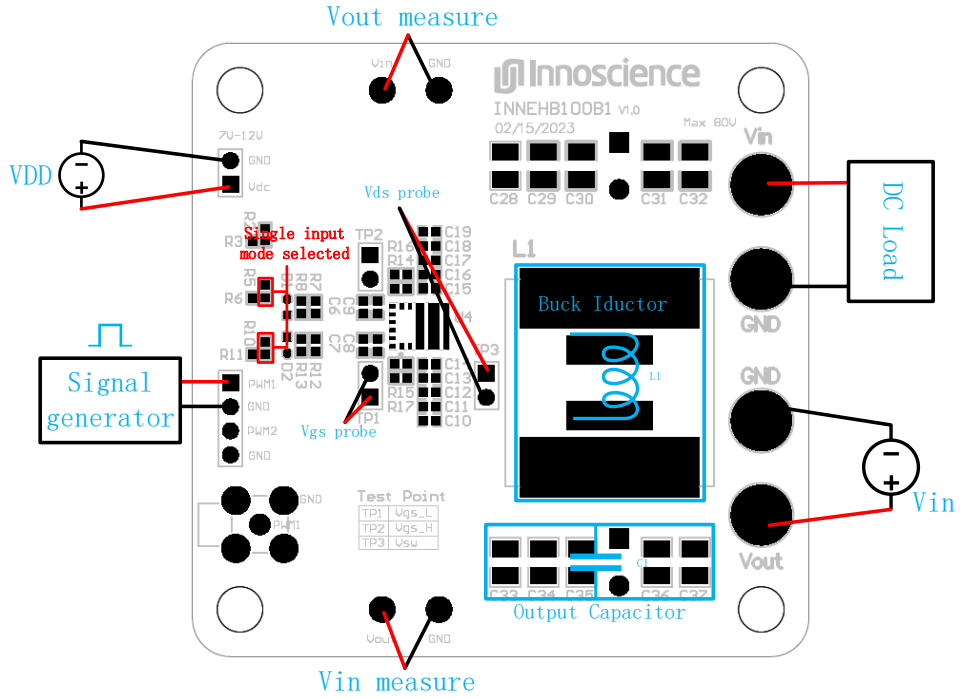


Figure 8 Single-PWM input Boost mode

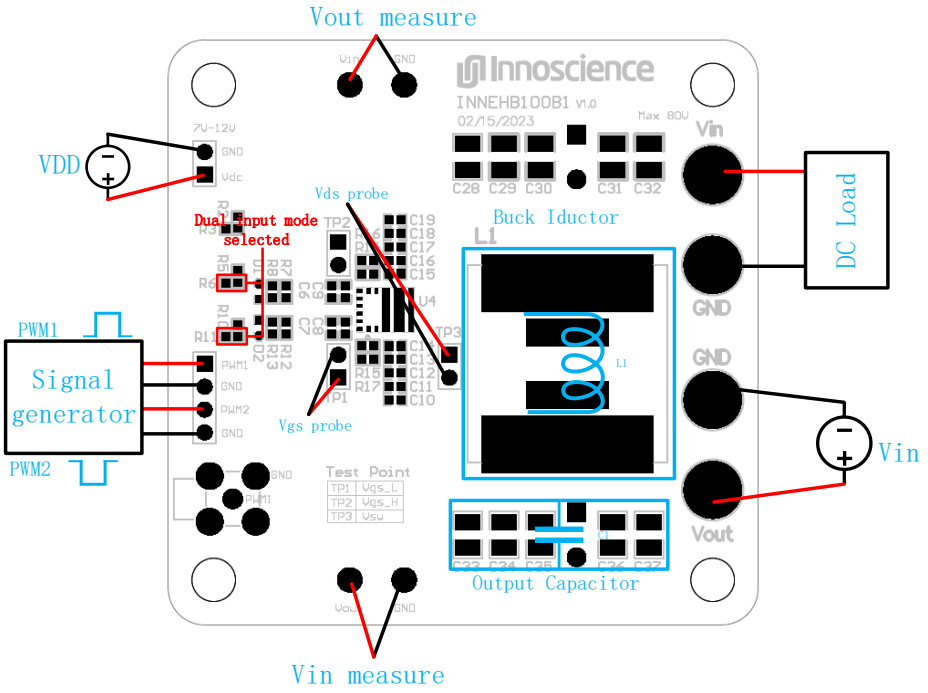


Figure9 Dual-PWM input Boost mode

5.3. Power up and down sequence

5.3.1. Power-up sequence (Buck Mode)

1. Ensure all the power supply are **off.**
2. Connect the DC voltage source to terminal **VIN** and common ground terminal **GND**, as shown in Figure 6 (Pay attention to the polarity).
3. Connect the electronic load to pin **VOUT.**
4. Connect the auxiliary power supply to the **VDD** terminal (Pay attention to the polarity).
5. Connect the signal generator to pins **PWM1** and **GND**.
6. Turn on the auxiliary power supply. Note the voltage ranges should be within 7V ~ 12V.
7. Turn on the signal generator and output the PWM signal with the required duty ratio and frequency.
8. Make sure the initial input supply voltage is 0 V, turn on the power and slowly increase the voltage to the desired value (do not exceed the absolute maximum voltage). Put the probes between switch-node and GND to measure the switching waveforms.
9. Slowly increase the load current according to the thermal status of the devices. Do not exceed the maximum temperature required by the device specification.

5.3.2. Power-up sequence (Boost Mode)

1. Ensure all the power supply is **off**
2. Connect the DC voltage source to the **VOUT** terminal, as shown in Figure 8 (Pay attention to the polarity).
3. Connect the positive terminal of the electronic load to **VIN** and the negative terminal to **GND**.
4. Connect the auxiliary source to the terminal **VDD** (Pay attention to the polarity).

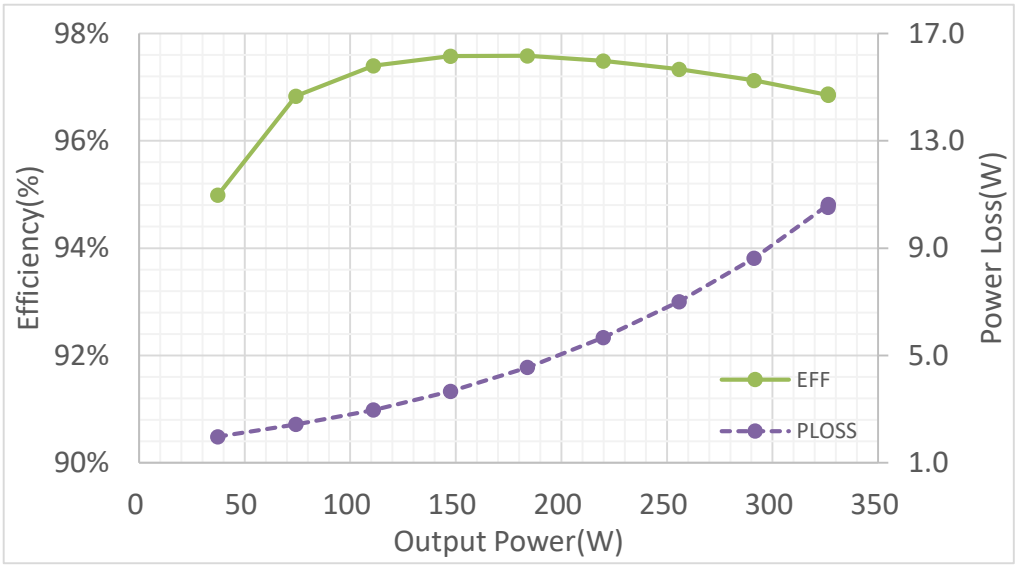
5. Connect the signal generator to pin **PWM1** and **PWM2,** and ground terminal **GND**.
6. Turn on the auxiliary power supply. Note the voltage ranges should be within 7V ~ 12V.
7. Turn on the signal generator and output the PWM signal with the required duty ratio and frequency.
8. Make sure the initial input supply voltage is 0 V, turn on the power and slowly increase the voltage to the desired value (do not exceed the absolute maximum voltage). Put the probes between switch-node and GND to measure the switching waveforms.
9. Slowly increase the load current according to the thermal status of the devices. Do not exceed the maximum temperature required by the device specification.

5.3.3. Power-down sequence

1. Turn off the **E-load** first
2. Turn off the **DC voltage source**
3. Turn off the **PWM generator**
4. Turn off the **auxiliary power supply**

6. Evaluation Results

6.1.1.Efficiency Results



Test conditions

Buck Mode

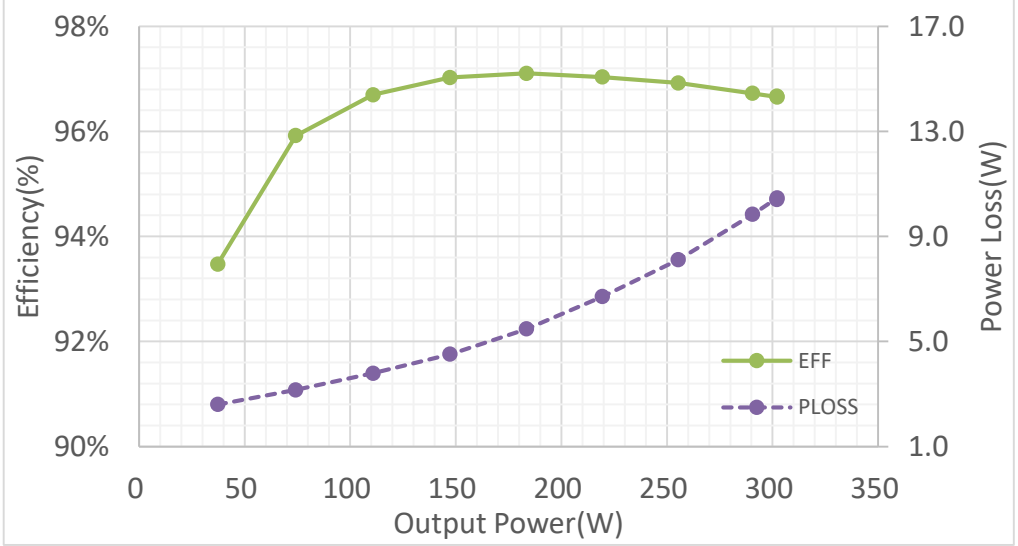
Vin=36Vdc

Vout=12Vdc

L=3.3uH

fsw=350kHz

Airflow=1400LFM



Test conditions

Buck Mode

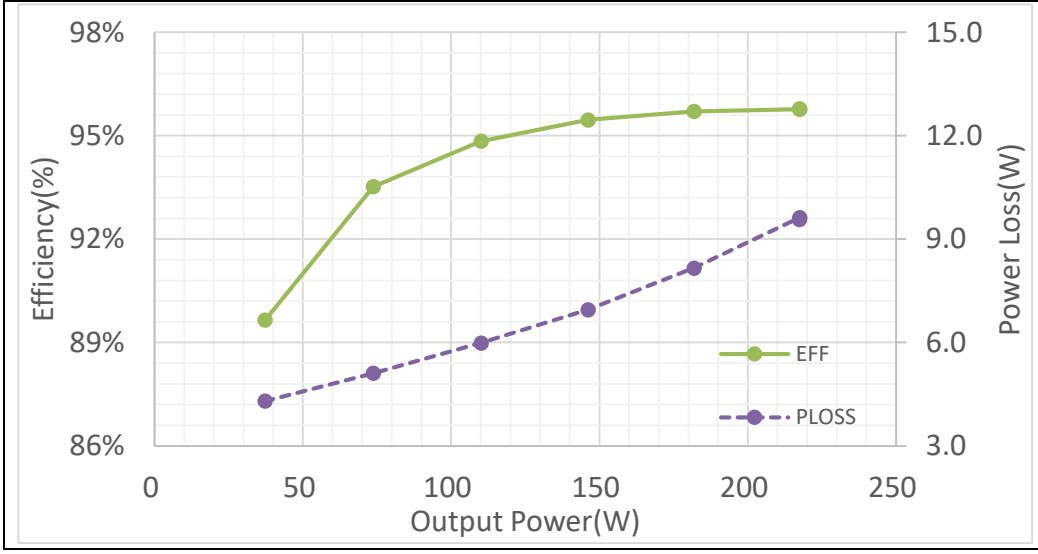
Vin=48Vdc

Vout=12Vdc

L=3.3uH

fsw=350kHz

Airflow=1400LFM



Test conditions

Buck Mode

Vin=80Vdc

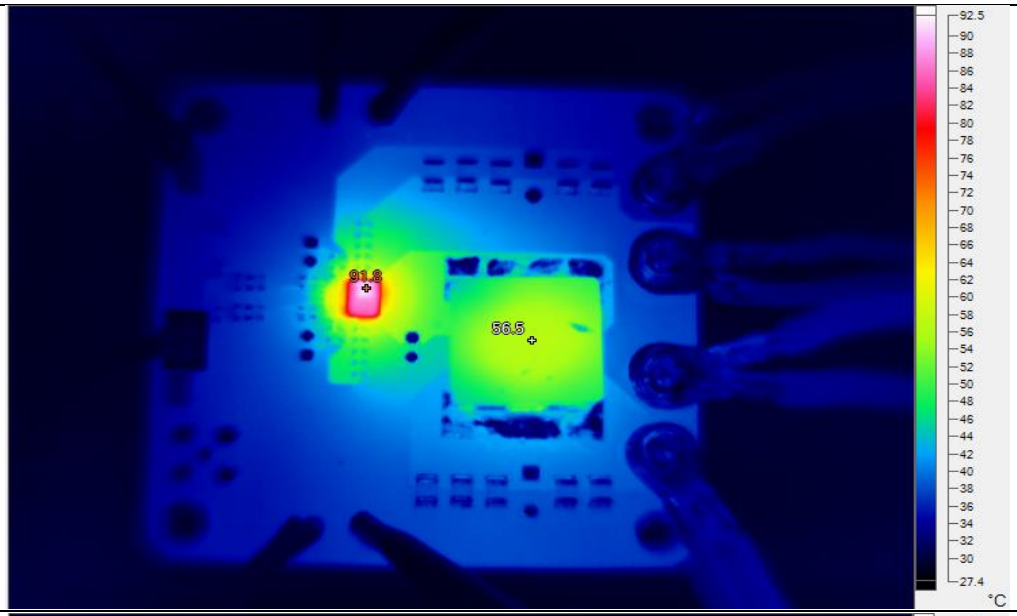
Vout=12Vdc

L=3.3uH

fsw=350kHz

Airflow=1400LFM

6.1.2.Thermal performance



Test conditions

Buck Mode

Vin=36Vdc

Vout=12Vdc

L=3.3uH

Iout=27A

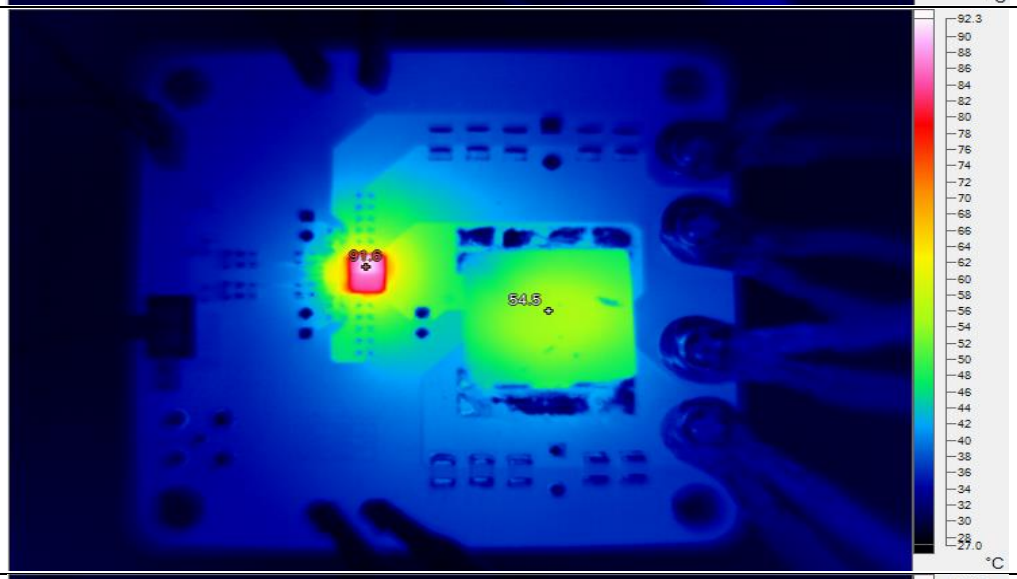
fsw=350kHz

Airflow=1400LFM

Result

SolidGaN: 91.8℃

Inductor: 56.5℃



Test conditions

Buck Mode

Vin=48Vdc

Vout=12Vdc

L=3.3uH

Iout=25A

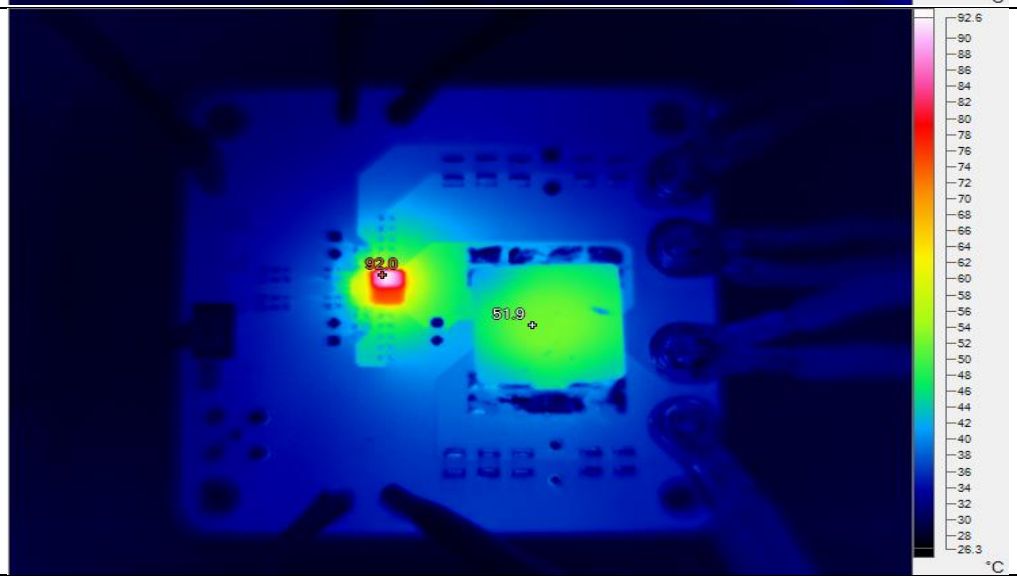
fsw=350kHz

Airflow=1400LFM

Result

SolidGaN: 91.6℃

Inductor: 54.5℃



Test conditions

Buck Mode

Vin=80Vdc

Vout=12Vdc

L=3.3uH

Iout=18A

fsw=350kHz

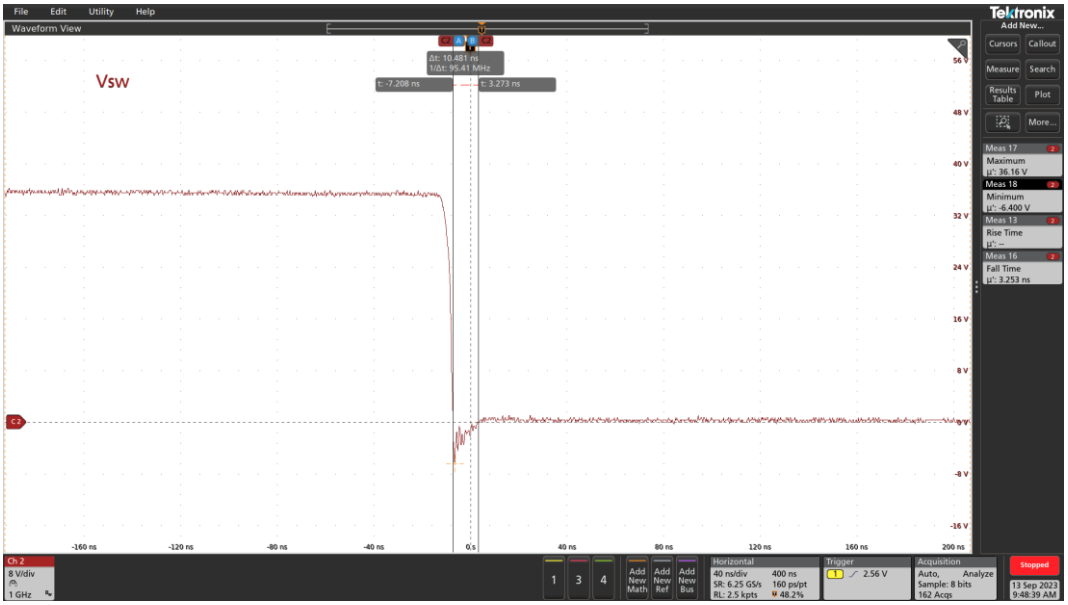
Airflow=1400LFM

Result

SolidGaN: 92.0℃

Inductor: 51.9℃

6.1.3.Switching Waveforms



Test conditions

Buck Mode

Vin=36Vdc

Vout=12Vdc

Iout=27A

fsw=350kHz

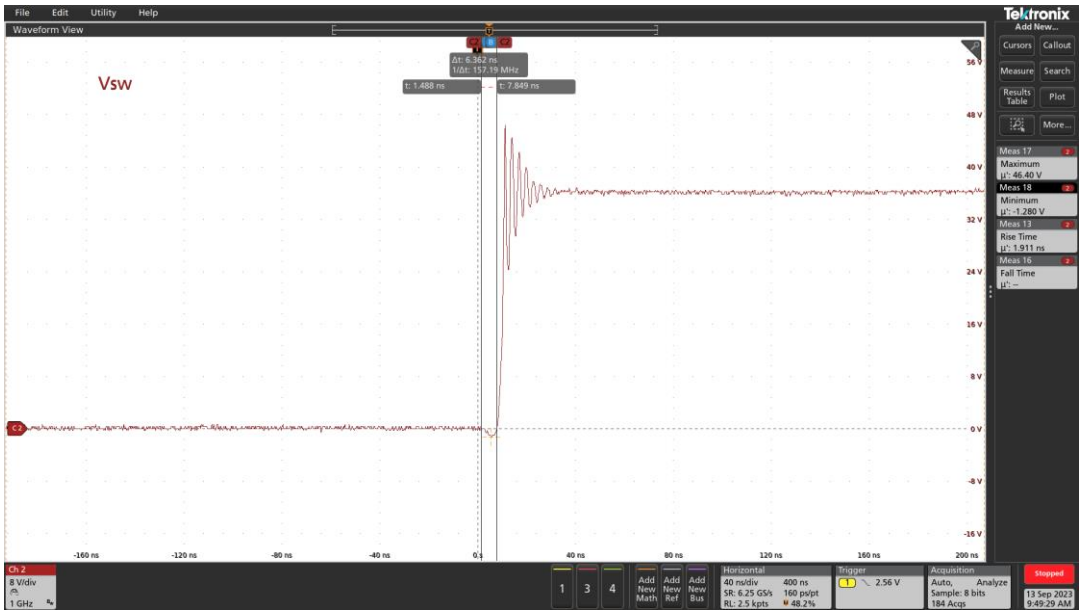
Airflow=1400LFM

Rg_on=3.6Ω

Result

SW Edge:

Falling time=3.253ns



Test conditions

Buck Mode

Vin=36Vdc

Vout=12Vdc

Iout=27A

fsw=350kHz

Airflow=1400LFM

Rg_on=3.6Ω

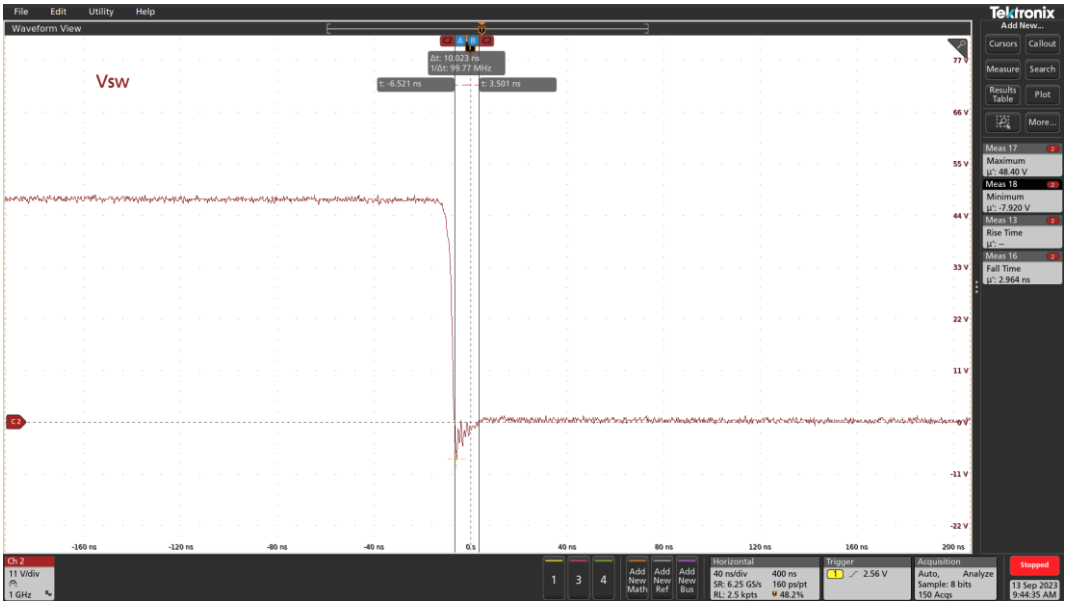
Result

SW Edge:

Rising

Overshoot=10.4V

Rising time=1.911ns



Test conditions

Buck Mode

Vin=48Vdc

Vout=12Vdc

Iout=25A

fsw=350kHz

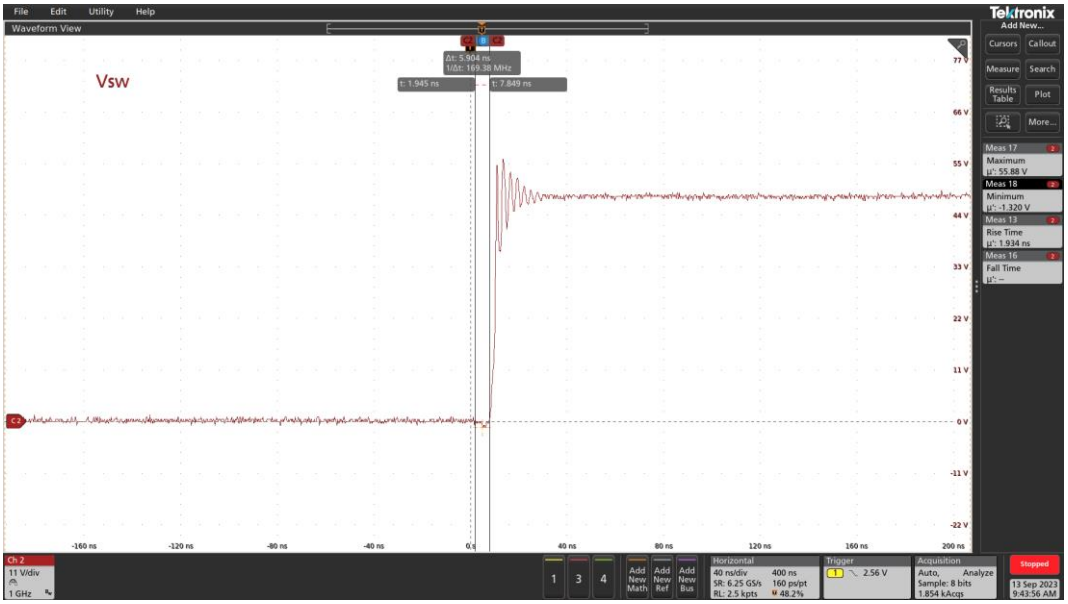
Airflow=1400LFM

Rg_on=3.6Ω

Result

SW Edge:

Falling time=2.964ns



Test conditions

Buck Mode

Vin=48Vdc

Vout=12Vdc

Iout=25A

fsw=350kHz

Airflow=1400LFM

Rg_on=3.6Ω

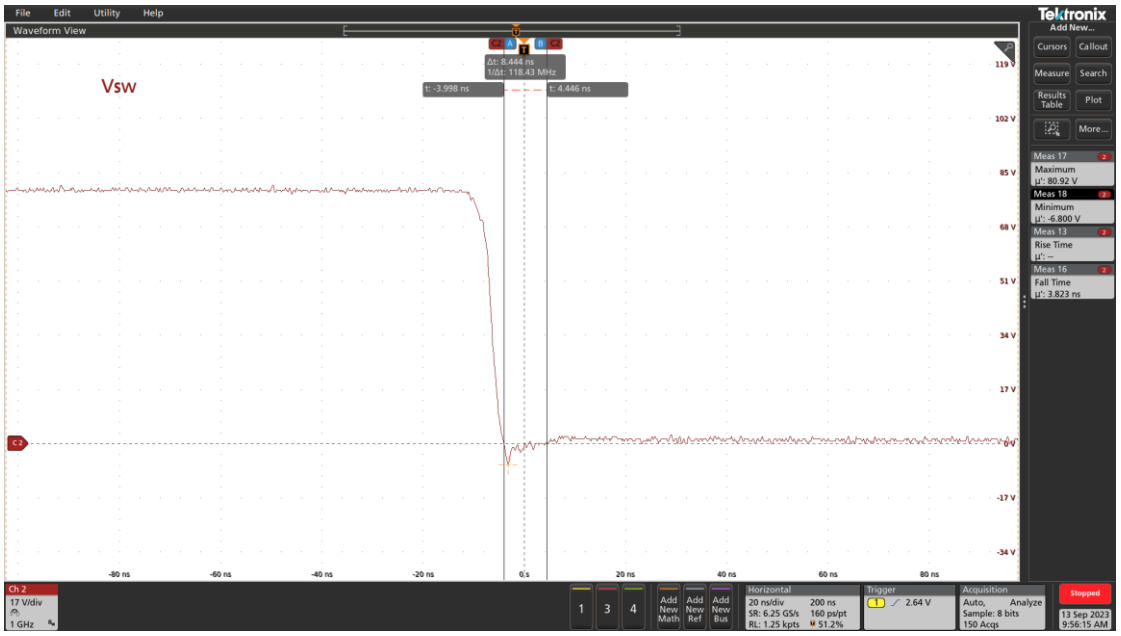
Result

SW Edge:

Rising

Overshoot=7.88V

Rising time=1.934ns



Test conditions

Buck Mode

Vin=80Vdc

Vout=12Vdc

Iout=18A

fsw=350kHz

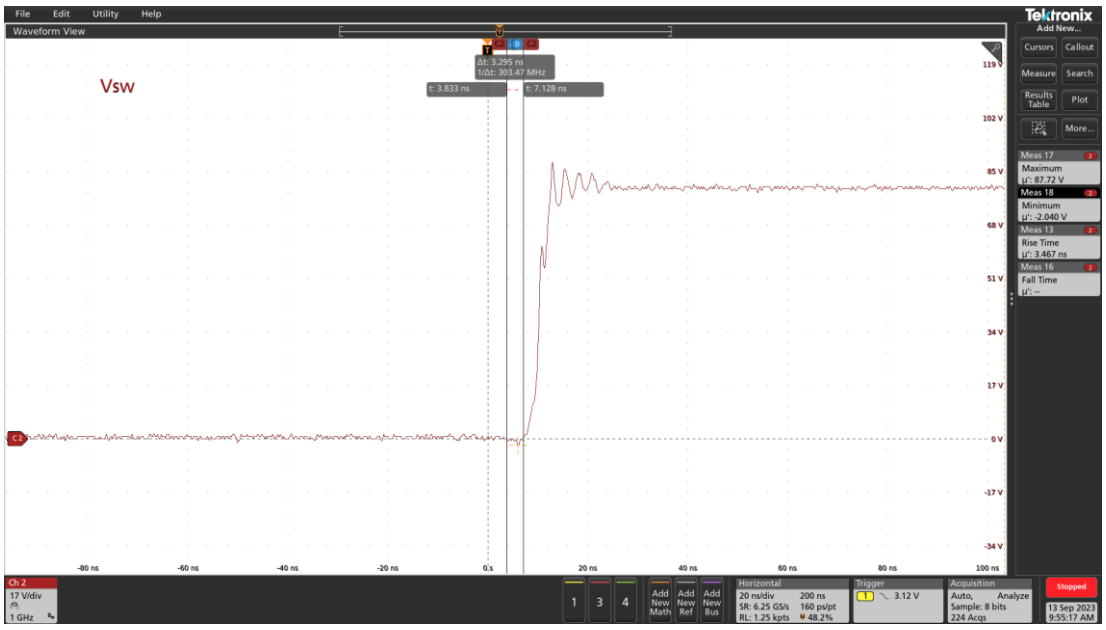
Airflow=1400LFM

Rg_on=3.6Ω

Result

SW Edge:

Falling time=3.823ns



Test conditions

Buck Mode

Vin=80Vdc

Vout=12Vdc

Iout=18A

fsw=350kHz

Airflow=1400LFM

Rg_on=3.6Ω

Result

SW Edge:

Rising

Overshoot=7.72V

Rising time=3.467ns

Appendix

Appendix A. PCB Layout

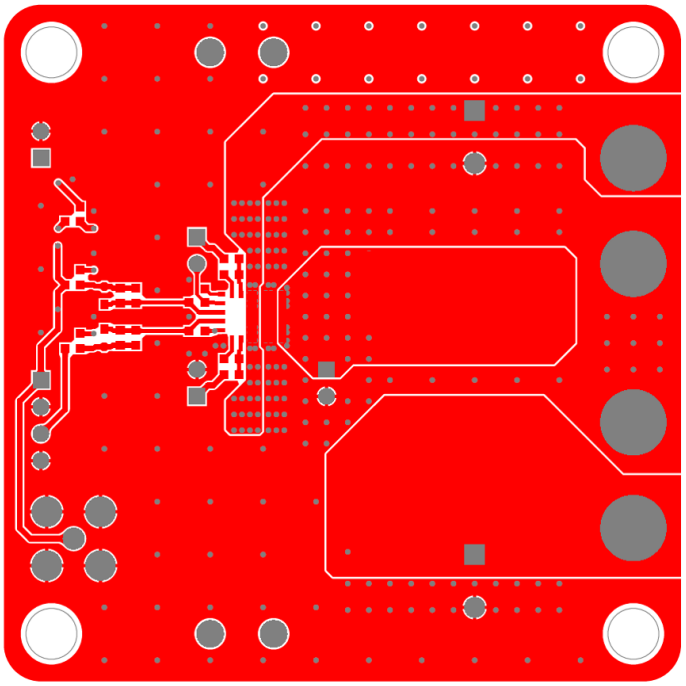


Figure 10 The top layer of INNEHB100B1

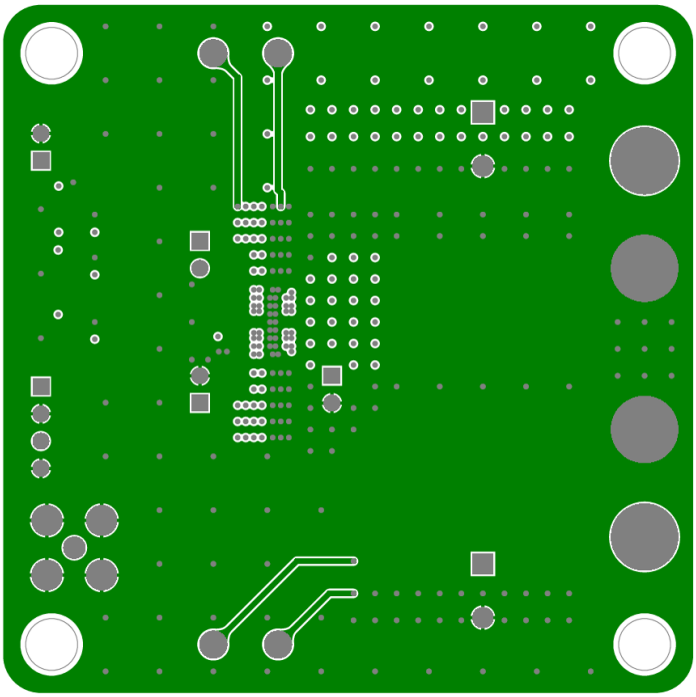


Figure 11 The first middle layer of INNEHB100B1

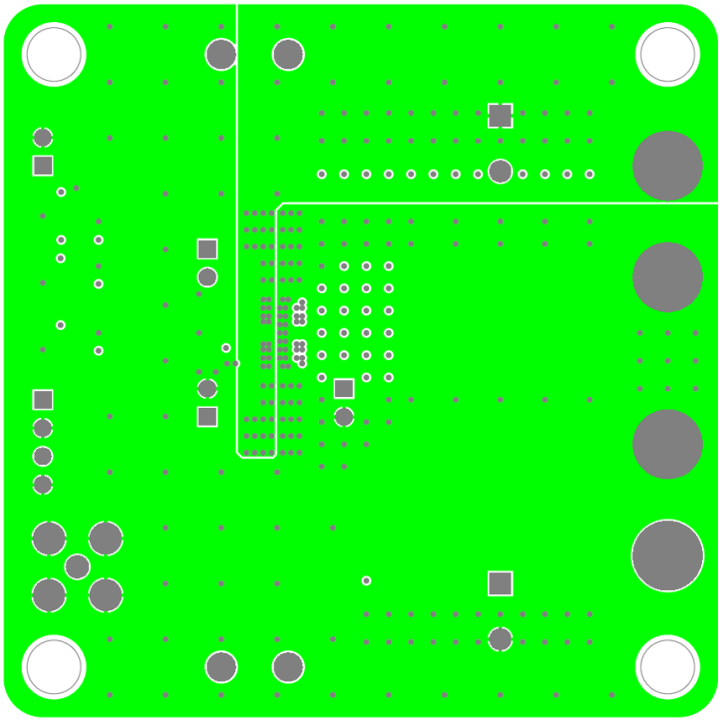


Figure 12 The second middle layer of INNEHB100B1

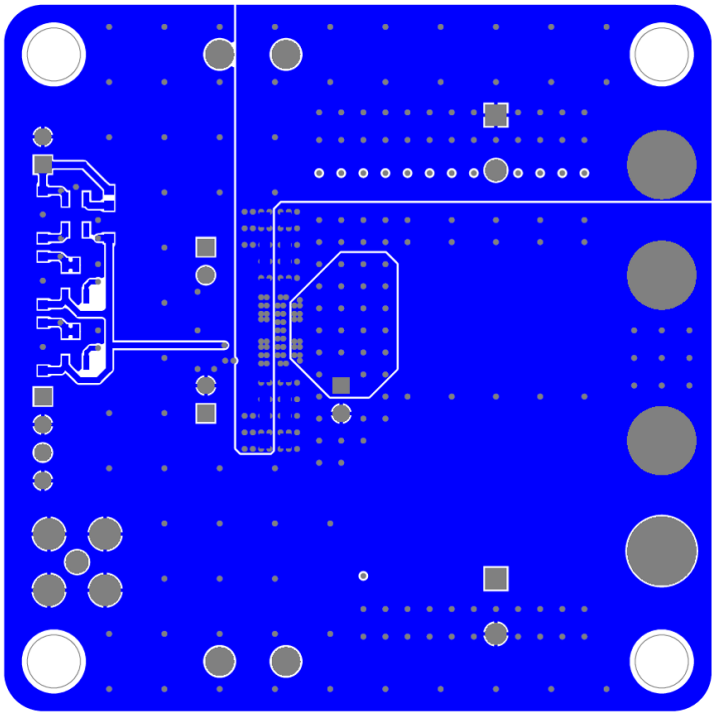


Figure 13 The bottom layer of INNEHB100B1

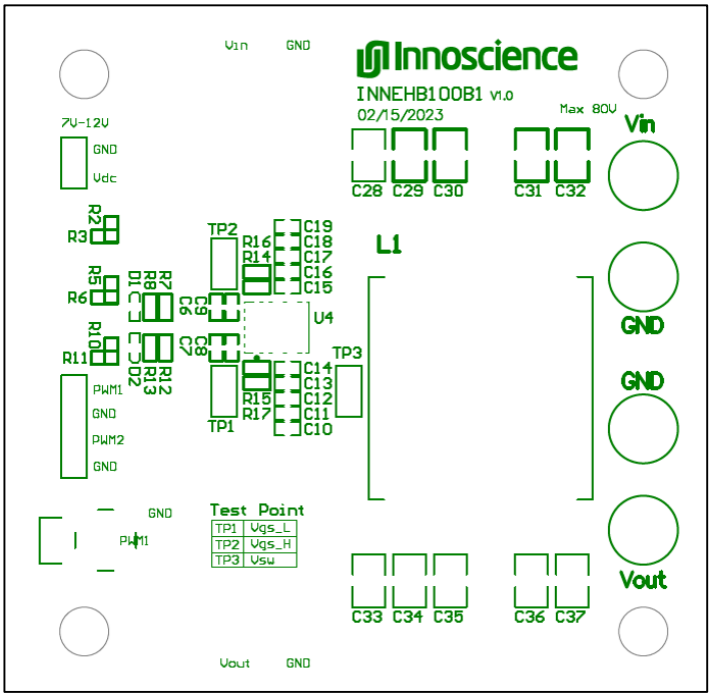


Figure 14 The top overlay of INNEHB100B1

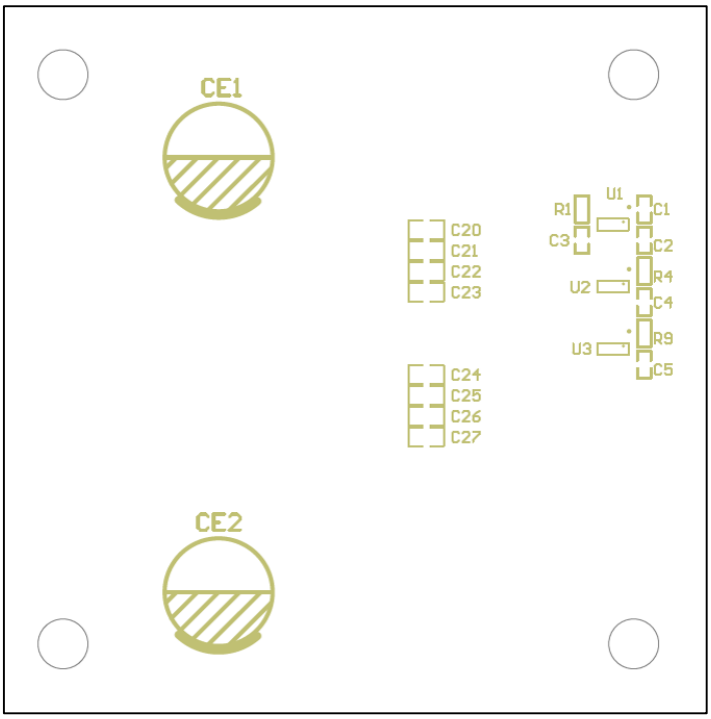


Figure 14 The bottom overlay of INNEHB100B1

Appendix B. BOM

Table 2 BOM

Designator	Part Number	Manufacturer	Description	Footprint	Quantity
C1, C3	CL10B105KA8NNNC	SAMSUNG	Cap, 1uF, X7R, 25V, 10%	C0603	2
C2, C8	GRM188R61E225KA12D	Murata	Cap, 2.2uF, X7R, 25V, 10%	C0603	2
C4, C5, C9	CC0603KRX7R9BB104	YAGEO	Cap, 0.1uF, X7R, 50V, 10%	C0603	3
C6, C7	CC0603JRNPO9BN101	YAGEO	Cap, 100pF, NPO, 50V, 5%	C0603	2
C10, C11, C12, C13, C14, C15, C16, C17, C18, C19	CL10B104KC8NNNC	SAMSUNG	Cap, 0.1uF, X7R, 100V, 10%	C0603	10
C20, C21, C22, C23, C24, C25, C26, C27	C0805X105K101T	Holy Stone	Cap, 1uF, X7R, 100V, 10%	C0805	8
C28, C29, C30, C31, C32	C3225X7S2A475K200AB	TDK	Cap, 4.7uF, X7S, 100V, 10%	C1210	5
C33, C34, C35, C36, C37	CL32B475KBJNFNE	SAMSUNG	Cap, 4.7uF, X7R, 50V, 10%	C1210	5
CE1, CE2	optional		Cap, optional, ϕ10mm		2
R1, R3, R5, R10, R16, R17	0603WAF0000T5E	UNI-ROYAL	Res, 0R, 1%, 0.1W	R0603	6
R2, R6, R8, R11, R13	optional	YAGEO	Res, optional	R0603	5
R4, R9	0603WAF1002T5E	UNI-ROYAL	Res, 10k, 1%, 0.1W	R0603	2
R7	0603WAF750JT5E	UNI-ROYAL	Res, 75R, 1%, 0.1W	R0603	1
R12	0603WA2700T5E	UNI-ROYAL	Res, 270R, 1%, 0.1W	R0603	1
R14, R15	0603WAF360KT5E	UNI-ROYAL	Res, 3R6, 1%, 0.1W	R0603	2
L1	MWLA1707S-3R3MT	Sunlord	3.3uH,45A	17mm x17.5mm x7mm	1
D1, D2	SDM03U40-7	Diodes	Schottky, 30V, 30mA, SOD-523	SOD-523	2
U1	SGM2210-5.0	SGMICRO	LDO, 5V, 300mA, SOT-23-5	SOT-23-5	1
U2	SGM7SZ08YN5G/TR	SGMICRO	AND Gate, 1.65V~5.5V, SOT-23-5	SOT-23-5	1
U3	SGM7SZ00YN5G/TR	SGMICRO	NAND Gate, 1.65V~5.5V, SOT-23-5	SOT-23-5	1
U4	ISG3201	INNOSCIENCE	SolidGaN, 100V/3.2mΩ*2, LGA 5x6.5	LGA 5mmx6.5mm	1
M1, M2, M3, M4	SMTSO3040CTJ	Sinhoo	Terminal, 30A, SMD M3x4	SMD M3x4	4

Revision History

Date	Author	Versions	Description	Check
2023/9/13	YubinHuang	1.0	First edition	AE Team

Note:
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